

Midterm Examination

You may **NOT** use any books or notes.
Be brief: Do what exactly you are asked.
Be neat.
And be lucky.

Name	Student#	Score

Problem 1. Convert the decimal number **43.28125** into IEEE floating-point standard 754 32-bit representation. The final representation must be an 8-digit hexadecimal number.

Requirement: You need to show **every step in detail**, including all the step-by-step conversion(s) – decimal to/from binary (if any), binary to/from hexadecimal (if any), excess 127 representation derivation (if any), etc. For example, when you are converting a decimal number to binary (if any), you cannot simply give the binary representation of a decimal number; you need show how you arrive at this binary representation.

Hint: The IEEE 754 32-bit representation uses 1 sign bit (0 for positive and 1 for negative), 8 exponent bits with excess 127 representation, and 23 fraction bits with implied “1.”. The number you are asked to represent is **not** any of the special numbers (like NAN or infinity).

The hexadecimal system uses the following digits to represent decimal numbers between 10 and 15: A–10, B–11, C–12, D–13, E–14, and F–15.

Problem 2 Assume we have the numbers represented in 5-bit two's complement forms. We have an addition given as follows.

$$\begin{array}{r} 10100 \\ + 11101 \\ \hline 10001 \end{array}$$

Verify the table actually gives the right answer by **answering** the following:

1. Does the overflow occur (yes/no)? _____;
2. The first operand represents decimal -12 (negative 12).
What's the decimal number the second operand represents? _____
3. What's the decimal number the result represents? _____

Problem 3 When you were space traveling, you encountered an alien document showing a table as follows. From other parts of the document, you (quite smartly!) deduced (1) that this was a multiplication table, (2) that this alien species actually used the radix 5 number system and (3) that they used following code to represent our decimal digits 0–4:

δ is 0, \dagger is 1, \ddagger is 2, @ is 3, \$ is 4

This table had some missing entries, and you were glad you took Dr. Wang's INFS515 towards the end of the 20th century (Earth time). Now **fill in the missing entries** as this is important for your mission.

*	δ	\dagger	\ddagger	@	\$
δ	δ	δ	δ	δ	δ
\dagger	δ	\dagger	\ddagger	@	\$
\ddagger	δ	\ddagger	\$		
@	δ	@		\dagger \$	\ddagger \ddagger
\$	δ	\$		\ddagger \ddagger	

Answer this: In this alien document, you saw the longest number has 2 digits (in radix 5 of course). You deduced (quite arrogantly!) that the largest number (in decimal) these aliens can think of is _____

Problem 4 The picture below shows the 8-way multiplexer, which has three “control” lines (A, B, C), and 8 inputs (D_0 – D_7), and one output (F). The function realized by this multiplexer is as follows: the input D_i is routed to the output F if and only if the number represented by the three-bit input A,B,C is i . For example, if A=1, B=C=0, then D_4 is routed to F, i.e., F takes the value of D_4 , since 100 in binary is 4 in decimal.

As we know, this multiplexer can be used to implement 3-variable Boolean functions (with A, B and C viewed as the three input variables, and F as the output) by wiring the input lines D_0 – D_7 appropriately to the ground or Vcc.

Problem 4.1 Now implement the Boolean function that gives 1 if the input has exactly two 0s, and gives 0 otherwise. You need to (1) show the truth table for the function (the table has 8 rows as given below), and (2) wire the lines D_0 – D_7 to the ground or to Vcc, respectively, based on the table.

Table:

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Problem 4.2

Answer this: How many different 3-variable functions this 8-way multiplexer is capable of realizing using the above method (i.e., by connecting D_0 – D_7 to the ground and Vcc, respectively)?

Answer: _____

True or False: Using the above 8-way multiplexer, we can implement all possible three-variable Boolean functions.

Answer: _____

Problem 5 Consider the following diagram.

Legend



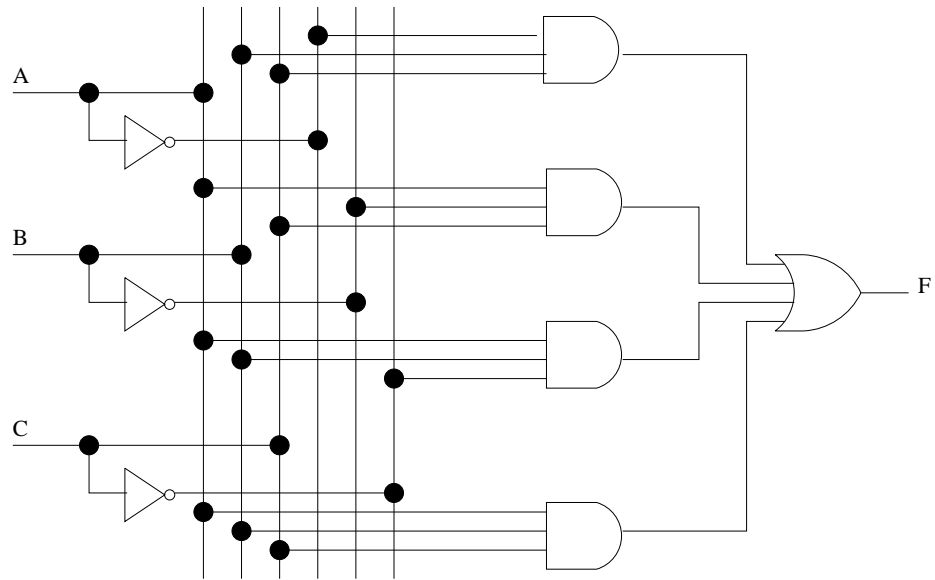
AND gate



OR gate



NOT gate



Give the truth table for what this circuit implements:

Problem 6 Assume there are two kinds of conditional instructions, *type1* and *type2*. Compare two 5-stage pipelined CPUs, CPU1 and CPU2. CPU1 stalls 3 cycles every time it hits a *type1* conditional instruction (but does not stall on any *type2*), while CPU2 stalls 4 cycles every time it hits a *type2* conditional instruction (but does not stall on any *type1*). Assume now there are 10 percent *type1* conditional instructions and 7 percent *type2* instructions. If a CPU takes a shorter time to execute 100 instructions (on average), then it's the better CPU.

Answer this: Which CPU is better (CPU1 or CPU2)? _____. Briefly explain why.

Problem 7 Assume all the gates in the following figures have a propagation delay of 10 nsec, and all other delays can be ignored. Consider the 8-bit ALU (composed of 8 1-bit ALU as shown).

Answer this: What is the earliest time the 8-bit ALU using this design can be sure of having outputs as all valid? Briefly explain why.

Hint: (1) There are two outputs from a 1-bit ALU: “carry out” and “output”. The time to get the “carry out” and the time to get the “output” may be different (look carefully at the left figure).
(2) Each 1-bit ALU (except for the rightmost one) needs the “carry out” signal from its right neighbor (not the “output” signal).

Problem 8 Briefly answer the following:

1. Give, in the correct order, the names of the main steps in the CPU execution cycle.

2. What's the purpose of PC (program counter) register in the CPU?

3. Everybody has the experience of operating a piece of machinery following a step-by-step instruction from a manual while holding the manual. Is it *interpretation* or *translation*?

4. Under which condition(s) cache is a good idea (circle all that apply):
 - (a) The cache memory is less expensive (in terms of "unit price") than the main memory.
 - (b) The cache memory is faster than the main memory.
 - (c) The accesses to memory locations by the CPU is totally random.
 - (d) The accesses to memory locations by the CPU stay in a limited part of the memory for extended periods.

5. Why are the memory locations usually organized into "lines" (each line consists of 4 to 64 consecutive bytes) as units for caches?

6. Assume a code has a minimum Hamming distance of 6 (i.e., for each pair of codewords in the code, the Hamming distance between them is at least 10). Is it true that it can be used to detect 6 bit errors (yes/no)? _____ Is it true that it can correct 2 bit errors (yes/no)? _____

7. A bus with bandwidth of 10Mbytes/second (each cycle the bus can transmit one byte, so it's running at 10MHz) is shared by disk (runs at 5Mbytes/second) and the CPU for them to access the main memory. What's the maximum speed the CPU can access the main memory if the disk is operating at its maximum speed? _____Mbytes/second.